IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	: 10/510,567	Confirmation No. :	9020
First Named Inventor	: Hirohisa MIYAZAWA		
Filed	: October 8, 2004		
TC/A.U.	: 2841		
Examiner	: TUAN T. DINH		
Docket No.	: 029267.55488US		
Customer No.	: 23911		
Title	: Circuit Board Device for Information Apparatus, Multilayered Module Board and Navigation System		

PRE-APPEAL BRIEF CONFERENCE REQUEST

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the Official Gazette noticed dated July 12, 2005, Applicant respectfully submits that the rejections of record are clearly not proper and without basis. As will be described in detail below, this Request is based on clear legal and factual deficiencies in the rejection, and is not based upon an interpretation of the claims or prior art teachings.

The Anticipation Rejection of Claims 1 and 5 by U.S. Patent No. 6,477,593 to Khosrowpour et al. ("Khosrowpour") Is Not Proper

A. The Rejection is Based Upon an Improper Application of the Law of Inherency

It is well established that anticipation requires an express or inherent disclosure of every claim element. Inherency requires that:

> the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established

> by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."[1]

The rejection of Applicant's claim 1 is relies upon inherency for the following claim elements:

1. a multilayer module board; and

2. a multilayer module board including at least a CPU and memory.

1. Khosrowpour Does Not Expressly or Inherently Disclose a Multilayer Module Board

The rejection of claim 1 relies upon daughterboard 120 as corresponding to the claimed multilayer board. The rejection, however, recognizes that there is no express disclosure in Khosrowpour that daughterboard 120 is a multilayer board. Instead, the Office Action states that daughterboard 120 is inherently a multilayer board, and cites U.S. Patent No. 5,025,306 to Johnson et al ("Johnson") to support this position on inherency.

Johnson does not, however, disclose that *all daughterboards must be multilayer boards*. Inherency has not been established merely because Johnson discloses that one type of daughterboard can be a multilayer board.

The rejection of claim 1 is for anticipation, and not obviousness. Thus, the rejection cannot be based upon a modification of Khosrowpour by Johnson or a combination of Khosrowpour and Johnson. Instead, the rejection can only rely upon the express or inherent disclosure of Khosrowpour. Johnson can only be relied upon to demonstrate that an inherent characteristic of Khosrowpour, i.e., that all daughterboards must be multilayer boards. Johnson does not.

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[1] M.P.E.P. § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Because the Office Action acknowledges that the express disclosure of Khosrowpour does not describe daughterboard 120 as a multilayer board, and Johnson does not prove that all daughterboards must be multilayer boards, the rejection of Applicant's claim 1 by reliance upon daughterboard 120 as corresponding to the claimed multilayer board is legally and factually deficient.

2. Khosrowpour Does Not Expressly or Inherently Disclose a Multilayer Module Board That Includes a CPU and Memory

The Response to Arguments section of the Office Action states that Figure 1 of Khosrowpour illustrates that daughterboard 120 includes a bigger chip, that corresponds to the claimed CPU, and three chips near the bigger chip that correspond to the claimed memory.

Khosrowpour does not, however, describe the type of chips mounted on daughterboard 120. Furthermore, there is nothing in the disclosure of Khosrowpour that would lead one of ordinary skill in the art to conclude that the bigger chip *must* be a CPU, or that the three other chips *must* be memories. Instead, it appears that the only basis for the interpretation of the bigger chip as being a CPU and the three other chips as being memories is the Examiner's opinion. Absent some express disclosure or other evidence establishing inherency of the bigger chip being a CPU and the three other chips being memories, the rejection being based solely on the Examiner's opinion is not legally or factually sufficient to establish anticipation of the claimed multilayer board containing a CPU and memory.

B. The Rejection Has Not Established that Khosrowpour Discloses The Type of Claimed Multilayer Board

Applicant's claim 1 recites that the multilayer module board mounted on a base board, and is one of a low-end module board, a high-speed module board or an advanced function module board.

Again, the rejection of claim 1 relies upon daughterboard 120 of Khosrowpour as disclosing the claimed multilayer board. Apart from describing the bus interface circuits and the composition of the boards themselves, Khosrowpour does not describe the type of function performed by daughterboard 120. Accordingly, Khosrowpour does not disclose that daughterboard 120 is one of a low-end module board, a high-speed module board or an advanced function module board. Nor does Khosrowpour disclose that motherboard 110 can accept more than one different type of board. In contrast, the base board of Applicant's claim 1 can accept a number of different types of multilayer module boards.

The Office Action has Not Established a *Prima Facie* Case of Obviousness of Claims 7-10 in View of the Combination of Khosrowpour and U.S. Patent No. 5,346,402 to Yasuho et al. ("Yasuho")

The Patent Office bears the initial burden of establishing a *prima facie* case of obviousness. This burden can only be established if the claim rejection provides evidence to support the obviousness of the claim elements.

The Office Action has not provided any evidence that the combination of Khosrowpour and Yasuho discloses or suggests the four connector terminals recited in claims 7-10.

As discussed in Applicant's Reply dated January 17, 2008, the rejection of claims 7-10 relies upon Yasuho for the disclosure of the claimed four connector terminals. The Office Action has not, however, indicated what portion of Yasuho discloses or suggests the claimed four connector terminals.

Applicant's Reply dated January 17, 2008, requested that the Patent Office provide a citation to Yasuho for the disclosure or suggestion of the claimed four connector terminals. Instead of providing such a citation, the Advisory Action merely states that the "Examiner maintains the final Office action mauled on 10/18/07." Thus, the Patent Office has not yet provided any evidence

that Yasuho discloses or suggests the claimed four connector terminals. Without any such evidence, the Patent Office has not yet established a *prima facie* case of obviousness.

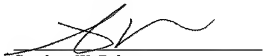
CONCLUSION

Because the Patent Office has not established that Khosrowpour expressly or inherently discloses the elements of claim 1, and the Patent Office has not met its burden in establishing a *prima facie* case of obviousness for at least claims 7-10, the rejections set forth in the final Office Action dated October 18, 2007, are factually and legally improper and must be withdrawn.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response, and please charge any deficiency in fees or credit any overpayments to Deposit Account No. 05-1323 (Docket # 029267.55488US).

Respectfully submitted,

February 19, 2008



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